IN THE CLAIMS

Please amend Claims 7, 8, 12, 20, 25, and 26 as follows:

Sub E1 A2

7. The system of claim 3, each of the first and second MOSFETs further comprising a respective PMOS transistor.

8. The system of claim 3, each of the first and second MOSFETs further comprising a respective NMOS transistor.

Sub E1 A3

12. The system of claim 1 defining a first system for extracting a threshold voltage, further comprising a second system for extracting a threshold voltage coupled to the first system for extracting a threshold voltage to provide a stacked threshold voltage extraction system having an output that is an integer multiple of the threshold voltage of the second system.

A4 Sub E1

20. The system of claim 16, the first and second parts of the voltage divider comprising first and second capacitors respectively.

Sub E1 A5

25. The system of claim 16 defining a first system for extracting a threshold voltage and further comprising a second system for extracting a threshold voltage coupled to the first system for extracting a threshold voltage to provide a stacked threshold voltage extraction system having an output that approximates an integer multiple of the threshold voltage of the second system.

26. The system of claim 16 in combination with a capacitor multiplier circuit, the combination comprising:

the capacitor multiplier circuit comprising first and second amplifier stages coupled together at a common node, the first stage having a first input that receives a bias current; and

the output voltage from the threshold voltage extraction system being applied to the capacitor multiplier circuit so that voltage approximately equal to the threshold voltage is at the common node, such that a startup offset for the capacitor multiplier circuit is mitigated as the bias current is applied to the first input of the capacitor multiplier circuit.